REMARKS

The present Amendment amends claim 1, 6-8, 10, 12, 14 and 18, leaves claims 3-5, 11, 13 and 17 unchanged, cancels claim 2 and adds new claims 19-27. Therefore, the present application has pending claims 1 and 3-27.

In paragraph 2 of the Office Action the Examiner alleges that the July 28, 2000 Information Disclosure Statement does not comply with the provisions of 37 CFR §1.97, 1.98 and MPEP §609. Applicants submit that the Examiner is in error in this regard being that the July 28, 2000 Information Disclosure Statement clearly complies with the rules. Particularly, the Examiner alleges that the listing of the references was not proper. In order to expedite matters, attached herewith is a Form PTO-1449 listing the references as encouraged by 37 CFR §1.98. However, the July 28, 2000 Information Disclosure Statement need not incorporate therein a concise explanation of the relevance of such references being that such concise explanation was provided in the Background of the Invention section of the present application on pages 2 and 3 thereof. Rule 37 CFR §1.98(a)(3)(i) which controls specifically states that:

> "the concise explanation may be either separate from Applicants specification or incorporated therein"

As can be seen above, no other requirements are set forth in the rules of practice which controls how Applicants are to respond. Further, the concise explanation of the relevance is only necessary when the references submitted are not in English. The references submitted with the July 28, 2000 Information Disclosure Statement were each in English or included an English language Abstract

which should have been considered by the Examiner. Thus, there is no need for a concise explanation of the relevance of the cited references. A copy of the references cited by the July 28, 2000 Information Disclosure Statement are attached herewith along with their English language Abstracts for consideration by the Examiner. It should be noted that with respect to Japanese patent application No. 5-225053 a corresponding U.S Patent was located, namely U.S. Patent No. 5,353,424. A copy of said patent is also provided and its number is listed on the attached PTO-1449. Therefore, Applicants submit that the Examiner was obligated to consider the references cited by the July 28, 2000 Information Disclosure Statement since these references each included an English language Abstract not requiring a concise explanation of the relevance thereof. An indication that the references have been considered is respectfully requested.

The specification stands objected to due to informalities noted by the Examiner. Particularly, the Examiner requested a new title indicative of the invention. The title of the invention was changed to "CACHE CONTROL METHOD AND APPARATUS IN A COMPUTER SYSTEM" which Applicants submit is descriptive of the present invention.

The Examiner also pointed to a misspelled word on page 22. The misspelled word was corrected. It should be noted that the specification was again reviewed so as to uncover any other minor errors grammatical and editorial in nature. However, no such other errors were uncovered. The Examiner is urged to identify any errors the Examiner may be aware of such that such errors can be immediately corrected.

Claims 1-18 stand rejected under 35 USC §102(b) as being anticipated by Tzeng (U.S. Patent No. 5,802,576) and claims 1-18 stand rejected under 35 USC §102(e) as being anticipated by Ramagopal (U.S. Patent No. 6,006,317). As indicated above, claim 2 was canceled. Therefore, this rejection with respect to claim 2 is rendered moot. These rejections with respect to the remaining claims 1 and 3-18 is traversed for the following reasons. Applicants submit that the features of the present invention as now recited in claims 1 and 3-18 are not taught or suggested by Tzeng or Ramagopal whether taken individually or in combination with any of the other references of record. Therefore, Applicants respectfully request the Examiner to reconsider and withdraw these rejections.

Applicants submit that the features of the present invention as recited in the claims are not taught or suggested by Tzeng or Ramagopal. The present invention as recited in the claims are directed to a coherent controller, which upon accepting a read request from a CPU, determines whether the request hits a cache or not and issues a speculative read request before a result of the cache hit or miss determination is issued. The coherent controller further issues a read request when the hit decision is a cache hit. In other words, the coherent controller in claim 1 is configured to not only issue a speculative read request to a cache data controller but also further issue a read request thereto if the cache is hit.

The claims now further define a structure of the speculative read request and a read request issued by the coherent controller. That is, the cache controller, upon accepting a speculative read request, reads data from a cache and holds the data in

hold means, and while accepting a read request, sends the speculative read data held in the hold means to the CPU as a reply data.

In claim 1, in parallel to the operation of a hit decision, reading of a cache data starts in response to the speculative read request without waiting for a result of hit decision is performed. Then, as a result of the hit decision (cache hit), a read request is newly issued so that the cache data previously read by the speculative read request is sent as the reply data. Thus, the hit decision operation and the cache data read operation are conducted in parallel, so that memory access latency may be hidden behind the hit decision operation.

Specifically, as explained in the Background of The Invention in the present specification, even when a cache tag portion and a cache data portion must be formed of separate LSIs through interfaces, the cache hit decision operation and the cache data read operation can be conducted in parallel to each other and independently from each other. Generally, as the capacity of the cache becomes large, the cache tag section needs to be held in a large-capacity, low-speed memory such as a DRAM. Therefore, memory access latency increases due to a DRAM read time in addition to a cache hit check time (process), to disadvantage. However, the above-mentioned parallel operation in this invention eliminates the disadvantage.

Tzeng does not disclose or suggest Applicants' features in claims 1 and 2 where a cache controller, upon accepting a read request from a CPU, determines a cache hit and issues a speculative read request before the decision of cache hit. The coherent controller further issues a read request when the hit decision is a cache

hit". Tzeng does not disclose the hold means and sending means as defined in the claims.

Rather, Tzeng discloses to write data DMA-transferred from a DMA device such as a disk drive into a L1 cache 24 and a L2 cache 20 in a microprocessor 10. In the DMA transfer an address 60 and a data stream 62 thereafter follow, as shown in Fig.3A. However, in the DMA transfer, only a starting address 60 is transferred, but a subsequent address is not transferred (col. 3, lines 13-20). The data length of the data stream is independent from the capacity of cache line and is generally greater than the cache line capacity. The data stream 60 is transferred through a buffer 34. The buffer 34 can hold 2 cache lines (col. 2, lines 52-56). Therefore, Tzeng, as shown in Fig.4, compares the starting address 60 to a cache tag (C), and if a cache hit occurs (D, F), one cache line is written into the L1 cache or the L2 cache. As to the subsequent data stream, since the subsequent address is not transferred, the address of the preceding cache line is incremented to determine the address of the subsequent cache line (K), and the step C is returned again to perform operation of the next cache line.

In Tzeng, as per col. 2, lines 1-6 pointed out by the Examiner, there is described that when a first line is written into a cache (from the buffer 34) , the next line can be accepted into the buffer 34 from PC bus 12 (that is, DMA device 18), and it can be decided whether the cache line is in the cache before the next line is accepted (into the buffer 34).

As is clear from the above, Tzeng discloses to check whether the next cache line is in the cache when a certain cache line is read or written (data 70 in Fig. 3A),

and then check whether the next cache line is in the cache (next subsequent cache line 74; snoop request control signal 72; and hit signal 76 in Fig. 3A). In other words, Tzeng discloses to read or write the cache line according to a decision of cache hit. This is apparent from the flowchart of Fig. 4. So, a cache is read or written according to step E of G after the cache hit decision in step D or F. As discussed previously, Tzeng does never teach Applicants' concept of "reading cache data without waiting for a result of cache hit or miss decision" anywhere of this patent.

Claim 6, of the present application defines a structure of storing a request to the same cache entry as an accepted speculative read request already into a speculative read request buffer.

Tzeng does teach or suggest such structural feature of not only issuing a speculative read request but also disregarding the accepted request as recited in claim 6 of the present application. Claim 11 is not taught by Tzeng for the same reasons as given to claim 1.

Thus, based on the above, Applicants submit that the features of the present invention as recited in the claims are not taught or suggested by Tzeng. Therefore, reconsideration and withdrawal of the 35 USC §102(b) rejection of claims 1-18 as being anticipated by Tzeng is respectfully requested.

Ramagopal, same as Tzeng appear to disclose a speculative store to a cache, that is, a write operation to the cache. Ramagopal does not teach or suggest the speculative read, that is, a read operation to a cache as recited in the claims of the present application. The alleged speculative store in Ramagopal is entirely different from the speculative read to a cache as recited in the claims.

In detail, as disclosed in col. 2, lines 20-32 and col. 5, lines 8-37 Ramagopal relates to a cache control for high-speed operation using an advanced control of instruction in a microprocessor. The advanced control predicts one of branch success and branch miss for an incoming branch instruction and proceeds to execute the predicted instruction stream. In col. 2, lines 20-32 of Ramagopal, this is called "speculative execution". In the speculative execution, a "store memory access" is not executed. In other words, since a write operation into memory rewrites an original data, recovery is not possible if mispredict branch occurs.

In col. 3, lines 63 to col. 4, line 18 of Ramagopal the Examiner cites, there is disclosed that in a speculative execution, cache data can be made recoverable even if a mispredict branch in the cache store operation occurs. When Ramagopal receives a selected store memory access, a first data (original data) of a given cache line is read out and a second data (rewritten data) is stored. The first data is stored in a second buffer for use upon occurrence of a mispredict branch. When the selected store memory access is incorrectly executed in the mispredict branch, the first data is returned back to the original cache line (col. 4, lines 10-18) of Ramagopal. As a result, even if store operation is executed upon speculative execution or mispredict branch, the cache can recover the original cache data. Thus, Ramagopal does not teach or suggest cache speculative read as recited in the claims of the present application. Ramagopal does not teach or suggest the features of the present invention as recited in the claims of a cache controller, upon accepting a read request from a CPU, determines whether the read request is a cache hit or a cache miss and issues a speculative read request without waiting for a result of the

determination, wherein the coherent controller issues a read request when the determination result is a cache hit.

Thus, as is quite clear from the above, the features of the present invention are not taught or suggested by Ramagopal. Therefore, reconsideration and withdrawal of the 35 USC §102(e) rejection of claims 1-18 as being anticipated by Ramagopal is respectfully requested.

As indicated above, the present Amendment adds new claims 19-27. New claims 19-27 recite many of the same features shown above not to be taught or suggested by Tzeng or Ramagopal. Particularly, new claims 19-27 define that the cache includes a cache tag section and a cache data section which operate independently from each other. The coherent controller refers to the cache tag section in response to a read request from the CPU to decide whether the read request is a cache hit or a cache miss. In response to a read request from the CPU the coherent controller issues a speculative read request before deciding whether the read request is a cache hit or a cache miss. In response to a decision of cache hit the coherent controller issues a. read request. The cache data controller, in response to a speculative read request from the coherent controller, reads a cache data from the cache data section and holds the read data into a hold buffer. The cache data controller further in response to the read request from the coherent controller, sends the cache data held in the hold buffer (means) as a reply data.

Thus, Tzeng and Ramapogal fail to teach or suggest the structural features of the present invention as recited in claims 19-27 the same as claims 1 and 3-18.

The remaining references of record have been studied. Applicants submit that they do not supply any of the deficiencies noted above with respect to the references utilized in the rejection of claims 1-18.

In view of the foregoing amendments and remarks, Applicants submit that claims 1 and 3-27 are in condition for allowance. Accordingly, early allowance of claims 1 and 3-27 is respectfully requested.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (500.38828X00).

Respectfully submitted,

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